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ORIGINAL ARTICLE

Performance improvements in complementary metal oxide semiconductor devices and circuits based on fin field-effect transistors using 3-nm ferroelectric $Hf_{0.5}Zr_{0.5}O_2$

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Abstract In this work, a conventional HfO_2 gate dielectric layer is replaced with a 3-nm ferroelectric (Fe) HZO layer in the gate stacks of advanced fin field-effect transistors (FinFETs). Fe-induced characteristics, e.g., negative drain induced barrier lowering (N-DIBL) and negative differential resistance (NDR), are clearly observed for both p- and n-type HZO-based FinFETs. These characteristics are attributed to the enhanced ferroelectricity of the 3-nm hafnium zirconium oxide (HZO) film, caused by Al doping from the TiAlC capping layer. This mechanism is verified for capacitors with structures similar to the FinFETs. Owing to the enhanced ferroelectricity and N-DIBL phenomenon, the drain current (I_{DS}) of the HZO-FinFETs is greater than that of HfO_2-FinFETs and obtained at a lower operating voltage. Accordingly, circuits based on HZO-FinFET achieve higher performance than those based on HfO_2-FinFET at a low voltage drain (V_{DD}), which indicates the application feasibility of the HZO-FinFETs in the ultra-low power integrated circuits.

Keywords FinFET; Ferroelectric; Hafnium zirconium oxide; Subthreshold swing; Low power

Introduction

Ferroelectric field-effect transistors (FeFETs) have the potential to achieve super-steep subthreshold swing (SS) or high driving currents suitable for ultra-low power consumption due to Fe dielectric layer induced negative capacitance and a high dielectric constant [1–4]. The most readily available Si complementary metal oxide semiconductor (CMOS)-compatible field-effect (FE) material is $Hf_xZr_{1-x}O_2$ (HZO), which has robust ferroelectricity and can be formed into thin films (< 20 nm), which may benefit scaling down of CMOS [5–7].

Recently, experimental evidence of performance enhancement and typical FE-induced characteristics, e.g., negative drain induced barrier lowering (N-DIBL), negative differential resistance (NDR), sub-60 $mV{\cdot}dec^{-1}$ of SSs, and improved on-state current have been reported for devices with thick HZO layers [8–13]. However, most typical characteristics are not obvious in advanced technology node logic devices based on ultra-thin HZO films in gate stacks, due to the weak ferroelectricity of thinner films. This effect has obstructed further exploration of super steep SS technology applied to advanced technology nodes [14–18]. Furthermore, although many experimental devices with HZO dielectrics have been reported, circuits based on FeFETs have rarely been demonstrated, and may yield improved performances on a circuit level [19–21].

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In this work, ferroelectric fin field-effect transistors (Fe FinFETs) and circuits using the main-stream "gate-last process" were fabricated with integration of a 3 nm ultra-thin HZO layer into the gate stacks. The enhanced ferroelectricity of the 3 nm HZO film caused by Al doping from the TiAlC capping layer contributed to obvious performance improvements in Fe FinFETs-based CMOS devices and circuits.

Experimental

The process flow that was used to fabricate FinFET devices and circuits with HZO and HfO_2 is illustrated in Fig. 1a. This basic process is similar to that used for developing n- and p-type devices on separate wafers [22, 23]. The FinFETs featuring a replacement metal gate were developed on the 200-mm Si (100) wafers. Initially, a self-aligned spacer image transfer technique was employed to pattern the fin morphology. Subsequently, standard procedures for punch-through stop doping (PTSD) and fin shallow trench isolation (STI) were adopted. Dummy gates constructed from amorphous silicon were fabricated using direct-write electron beam and dry etching techniques. After procedures for dummy gate planarization and removal had been carried out, atomic layer deposition (ALD) was applied to produce dual-work-function metal gates, which were used to set the threshold voltages (V_T) of the n- and p-type FETs after fabrication of the interfacial layer (IL) and high-k dielectric layer. The diagrams in Fig. 1b demonstrate the intricate layered films of the n- and p-type devices. The uniform 3 nm thick HZO and HfO_2 dielectric layers were produced through alternate incorporation of organic precursors based on Hf or Zr. The device contact processes for the source and drain (SD) W-plug and gate were applied to form the contact holes. Forming gas annealing (FGA) at 450 °C for 30 min was applied to the Al electrode of both devices with HZO crystallization.

Transmission electron microscope (TEM) imaging was used to examine the cross-sectional profiles of FinFETs. The electrical characterization was conducted using semiconductor parameter analyzers Keithley 4200 and Agilent 4156 C.

Results and discussion

Ferroelectricity enhancement of 3 nm HZO film

Figure 1c–e shows a schematic diagram, TEM images (cut across AA′), and energy dispersive X-ray spectroscopy (EDX) mappings of HZO-based FinFETs, respectively. Figure 1d shows that the fin had a top thickness of 4 nm and a height of approximately 70 nm. The interfacial layer (IL) and HZO layers were 1 and 3 nm thick, respectively, which gave superior gate control over the channel. Figure 1e shows the elements distribution of a p-type device, revealing the conformal work function metal layers around the entire 3D fins channel. Hf and Zr atoms concentrated in the medium layer, but Al diffused into the adjacent layers.

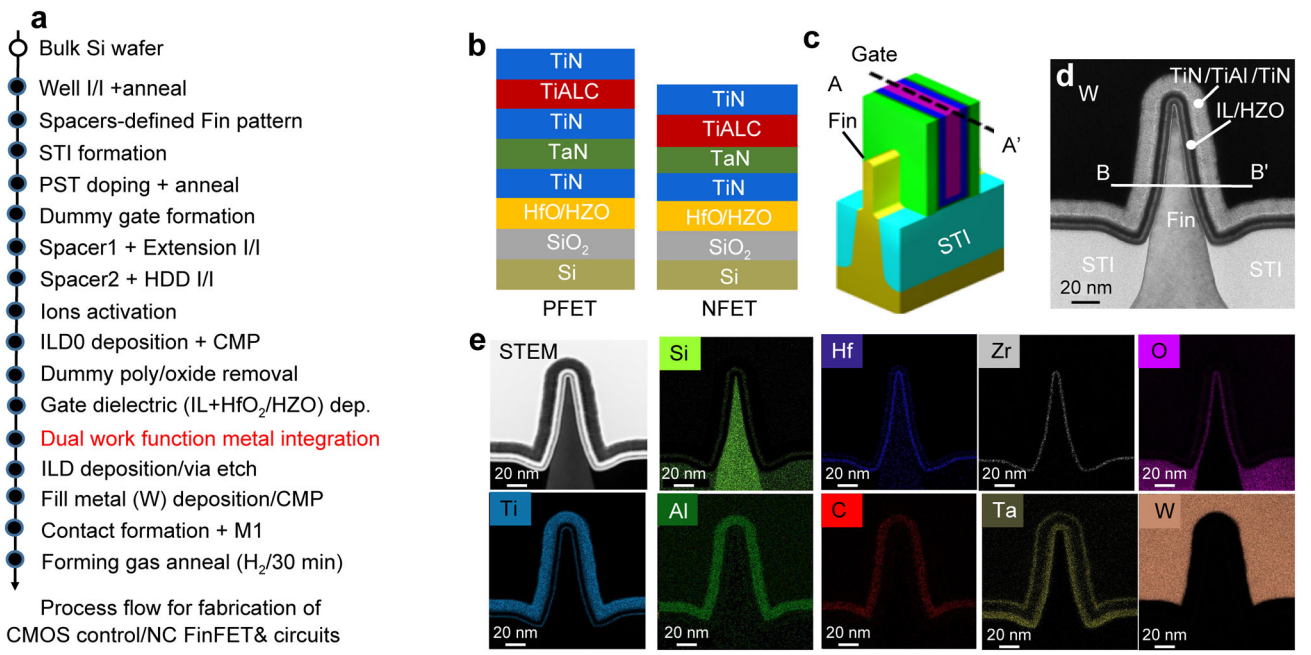

Fig. 1 **a** Fabrication process of FinFETs with a FE film replacing metal gate; **b** detailed gate stack layers of n- and p-type FET; **c** schematic diagram, **d** TEM image and **e** EDX mapping images of a p-FinFET with 3-nm HZO

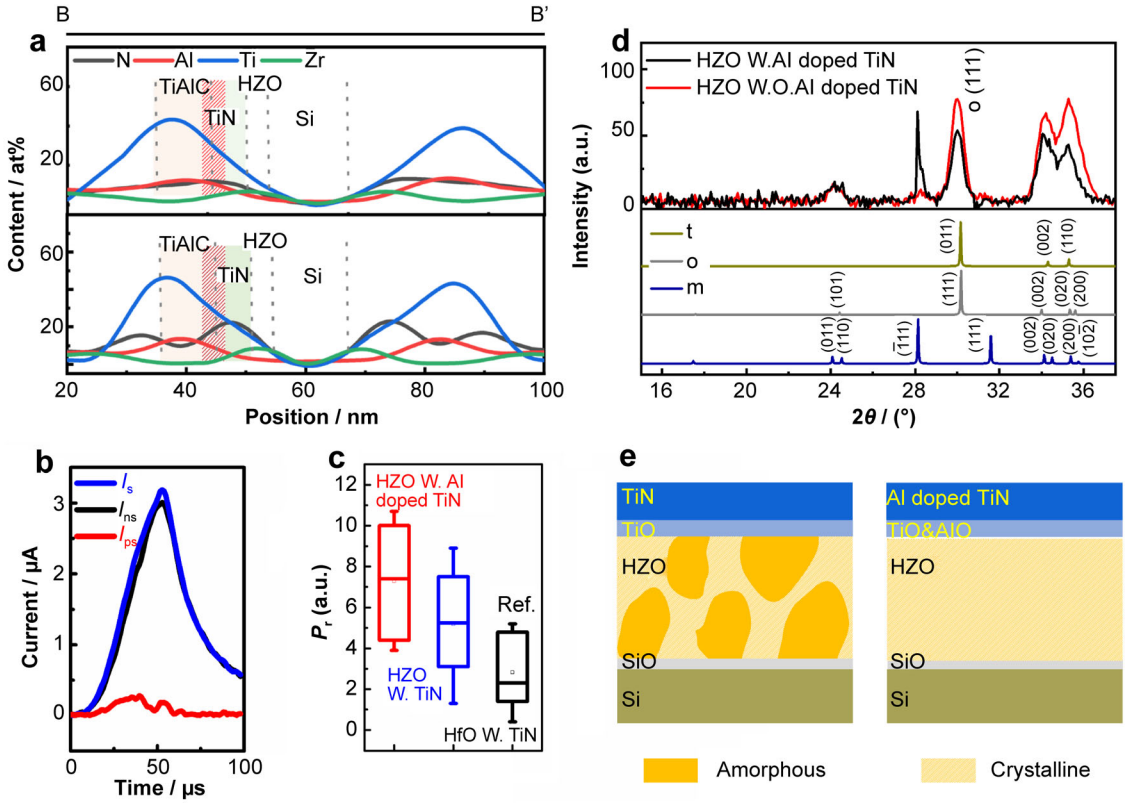

Fig. 2 **a** Corresponding line scan for N, Al, Ti and Zr, respectively; **b** PUND results of current signals of HZO-based capacitor with Al-doped TiN; **c** comparison of P_r from capacitors with HZO/Al-TiN, HZO/TiN, and HfO/TiN; **d** XRD patterns of samples with and without Al-doped TiN; **e** schematic diagram of interactions between HZO films and Al-doped TiN and TiN capping layers

To verify the elemental diffusion, the distribution of the elements in the devices is shown in Fig. 2a. Elemental line scans (along BB′ in Fig. 1d) indicate obvious diffusion of Al into the TiN layer to form Al-doped TiN due to the strong diffuse tendency of Al atoms (especially considering the annealing process at 450 °C).

Figure 2b shows positive-up-negative-down (PUND) results measured using a voltage pulse (1 V, 50 μs) on an HZO-based capacitor with a similar structure to the gate stacks of the HZO-based FinFETs. The polarization switching current (I_{ps}) and the non-switching current (I_{ns}), which was measured during the application of the second voltage pulse, constitute the transient current (I_s) arising from the application of the first voltage pulse [24]. By integrating the I_{ps} signal, which is the difference between I_s and I_{ns}, the remnant polarization values are obtained. Accordingly, a comparison of the capacitances based on 3 nm HZO with Al-doped TiN and TiN electrodes is identified, as shown in Fig. 2c. Compared with the capacitance of the device with a TiN electrode, an improvement in the P_r value of approximately 20% was obtained with the Al-doped TiN electrode. Figure 2d shows XRD patterns of the 3 nm HZO films with Al-doped TiN and TiN capping layers. The orthorhombic phase was confirmed in both films. Furthermore, consistent with the PUND results, for the Al-doped TiN capping layers, the (111) peak was sharp and intense, indicating good crystallinity and chemical ordering [25–27]. This result is mainly attributed to the presence of AlO_x at the interface that may facilitate HZO film crystallization, as shown in Fig. 2e, and has also been reported for other elemental oxides [28–30].

HZO-based devices results

The electrical characteristics of the FinFETs with 3-nm HfO and HZO were subsequently investigated. Figure 3a, c shows the transfer curves of both types of CMOS FinFETs at V_{DS} of |100| mV (LIN) and |800| mV (SAT), respectively. Unlike the devices based on HfO_2 as the dielectric layer, an obvious N-DIBL phenomenon was observed for the FinFET with 3-nm HZO due to its enhanced ferroelectricity. Importantly, owing to the N-DIBL effect, the I_{DS} in the subthreshold region of the HZO-based devices was much larger than that of the FinFETs with HfO_2.

To investigate the N-DIBL effects further, dual-sweep I_{DS}-V_{GS} curves were obtained over a range of V_{DS}, and the

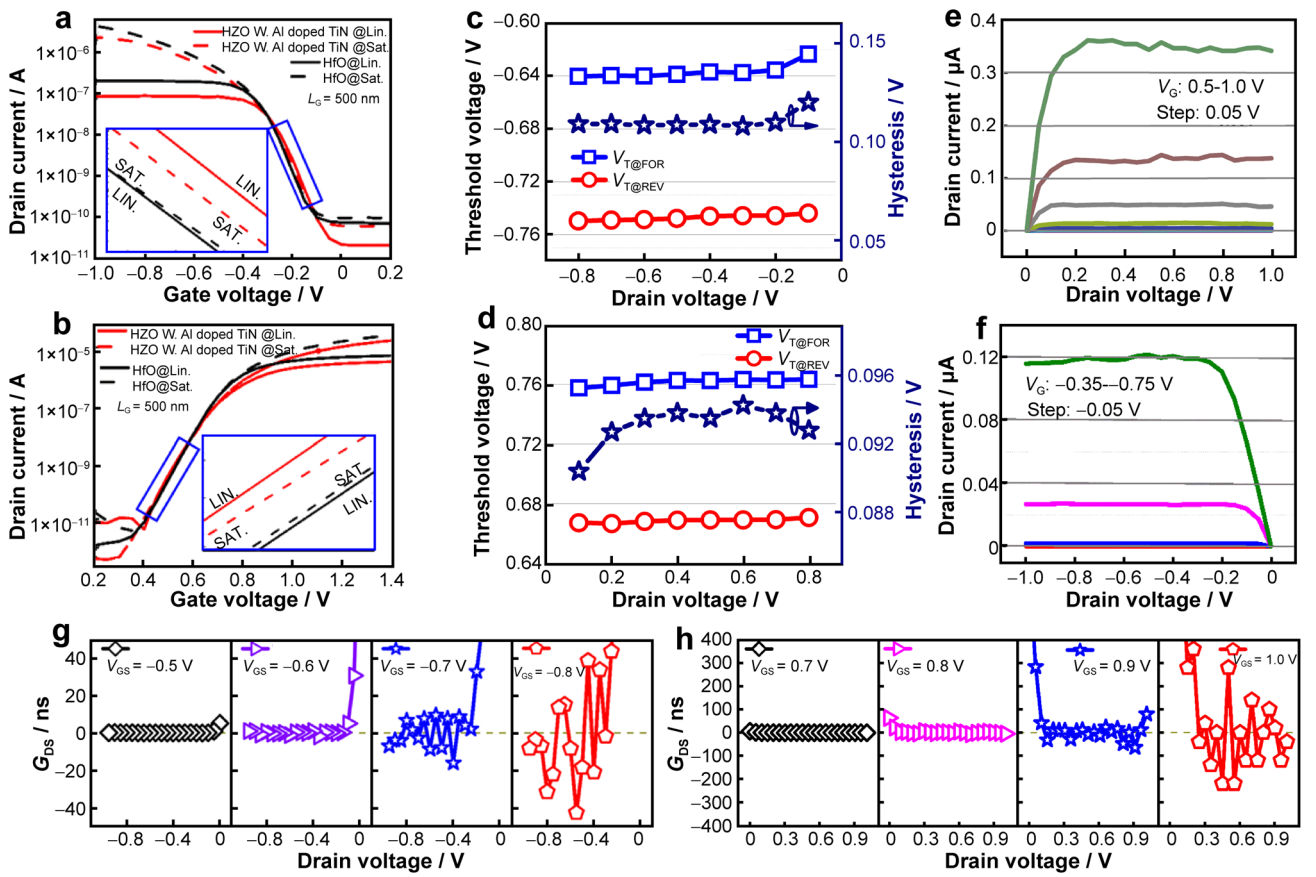

Fig. 3 **a** I_{DS}-V_{GS} curves of p-type HZO-based FinFET at various V_{DS}; **b** extracted V_T as a function of I_{DS} of device in **a**; **c** I_{DS}-V_{GS} curves of n-type HZO-based FinFET at various V_{DS}; **d** extracted V_T as a function of I_{DS} of device in **c**; measured I_{DS}-V_{DS} curves and NDR phenomenon of **e** n-type and **f** p-type FinFETs with 3-nm HZO; **g**, **h** extracted G_{DS} as a function of V_{DS} under various V_{GS} for p- and n-type HZO-based FinFETs in **e, f**

extracted V_T values for p- and n-type HZO-based FinFETs at various V_{DS} biases are shown in Fig. 3b, d, respectively. The values of the $V_{T@FOR}$ and $V_{T@REV}$ decreased (increased) as V_{DS} steadily increased for p-type (n-type) HZO-based FinFET, indicating the presence of the N-DIBL over almost the whole V_{DS} range. In addition, the hysteresis (defined as $V_{T@FOR} - V_{T@REV}$) was negligible and very stable. Specifically, the hysteresis was stable at $\sim$ 90 and $\sim$ 110 mV for the n- and p-type HZO-based FinFETs with different V_{DS}, respectively, which was much smaller than values of previously reported devices [21]. Furthermore, a clear negative differential resistance (NDR) stemming from the N-DIBL effect was also observed in the output curves of HZO-based CMOS devices (Fig. 3e, f for n- and p-type devices, respectively). In addition, the NDR phenomenon became more obvious at higher V_{GS}, which was consistent with the conclusions of previous theoretical predictions [9, 10]. The extracted differential resistance, defined as G_{DS}, as a function of V_{DS} curves is illustrated in Fig. 3g, h, indicating that HZO-FinFETs with 3 nm ultra-thin HZO have a negative G_{DS}. Specifically, for the p-type HZO-FinFET shown in Fig. 3g, when V_{GS} is less than − 0.5 V, a low negative G_{DS} occurs. As V_{GS} increases to − 0.6 V, partial G_{DS} values change from positive to negative. Notably, unlike the smooth G_{DS}–V_{DS} curves previously reported [9, 10], the G_{DS} values appeared to fluctuate around 0 at higher V_{GS}, which might indicate that the NC effect in this work was dynamic rather than static as previously reported [31–32]. Figure 3h shows that as V_{GS} increases to 0.9 V, the partial G_{DS} values also change from positive to negative in n-type devices which is consistent with the behavior of a p-type transistor.

Figure 4a shows the distribution of DIBLs for the HZO-based and HfO-based FinFETs over 60 devices. There are few N-DIBL characteristics for FinFETs based on conventional HfO_2 films. However, The N-DIBL phenomenon was observed for almost all HZO-based FinFETs, indicating good uniformity and stability of the devices. The median values of DIBLs were − 0.003 and 0.012 V for HZO- and HfO_2-FinFET devices, respectively. In addition

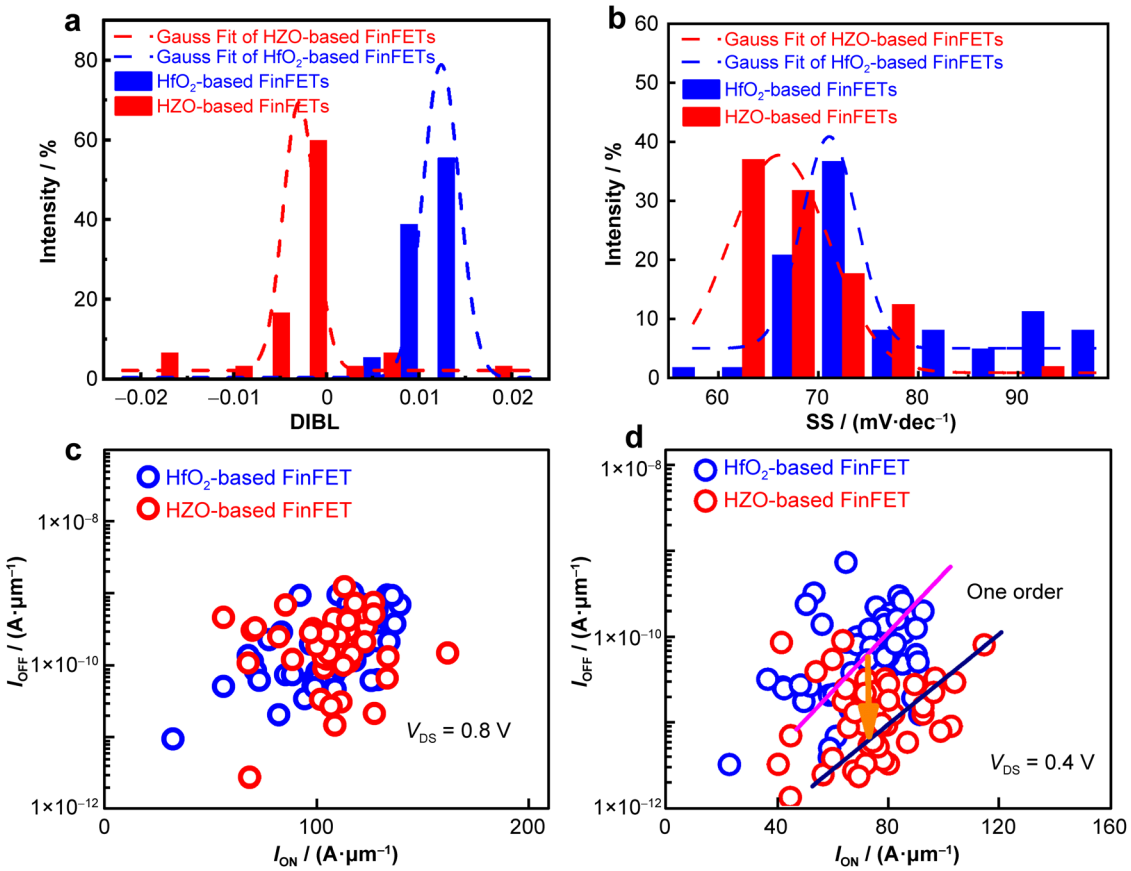

Fig. 4 **a** Distribution of DIBL values of HZO-based FinFETs and HfO_2-based FinFETs; **b** distribution of SS values of HZO-based FinFET and control FinFET; **c** I_{on}-I_{off} mappings for HZO-based FinFET and HfO_2-based FinFET at V_{DS} = 0.8 V; **d** I_{on}-I_{off} mappings for HZO-based FinFET and HfO_2-based FinFET at V_{DS} = 0.4 V

to N-DIBL and NDR, the ferroelectric effect was also reflected in the improved SS, as shown in Fig. 4b. Although the SSs of FinFETs with a 3 nm ultra-thin HZO layer did not exceed the limit of 60 mV·dec^{-1}, the sub-threshold voltage switching characteristics of HfO_2-based FinFETs were improved compared with those of the HfO_2-FinFETs. The SS distribution in Fig. 4b indicates that the median SS was approximately 67.5 mV·dec^{-1} for the HZO-based FinFETs and 79.7 for the HfO_2-based FinFETs mV·dec^{-1}. Therefore, a decrease in the average SS of ~12.2 mV·dec^{-1} was achieved for the Fe FinFETs.

Figure 4c, d shows I_{ON}-I_{OFF} distributions of HZO- and HfO_2-based FinFETs at 0.8 and 0.4 V V_{DD}, respectively. The performance of the two types of devices was almost the same when V_{DD} = 0.8 V. However, when V_{DS} was decreased to 0.4 V, the off-current of the HZO-based FinFET decreased by an order of magnitude compared to that of the FinFET with a 3-nm HZO at the same level of on-current. This result is attributed to the obvious FE effects.

HZO-based FinFET circuits results

Figure 5a shows typical voltage transfer curves (V_{TC}) of HZO- and HfO-based FinFETs CMOS inverters in a series of supply voltages. The maximum voltage gain of the two CMOS inverters exhibited little difference under high supply voltages. However, the voltage gain of the HZO-based FinFET inverter was greater than that of the controlled inverter when the supply voltage was lower than 0.6 V, which might have been caused by the higher I_{DS} at lower V_{DD}s due to N-DIBL phenomenon (Fig. 5b). These characteristics indicate the potential for the application of these devices in low-power integrated circuits. Additionally, Fig. 5d shows the output waveforms of 55-stage ring oscillators (ROs, Fig. 5c) for the HZO- and HfO-based FinFETs. The oscillation frequencies of the HfO-based and HZO-based FinFETs were 178 and 222 kHz, respectively. Owing to the performance of the HZO-based FinFETs, a 19.9% increase in oscillation frequency and a 16% reduction in delay per stage were achieved for the HZO-based

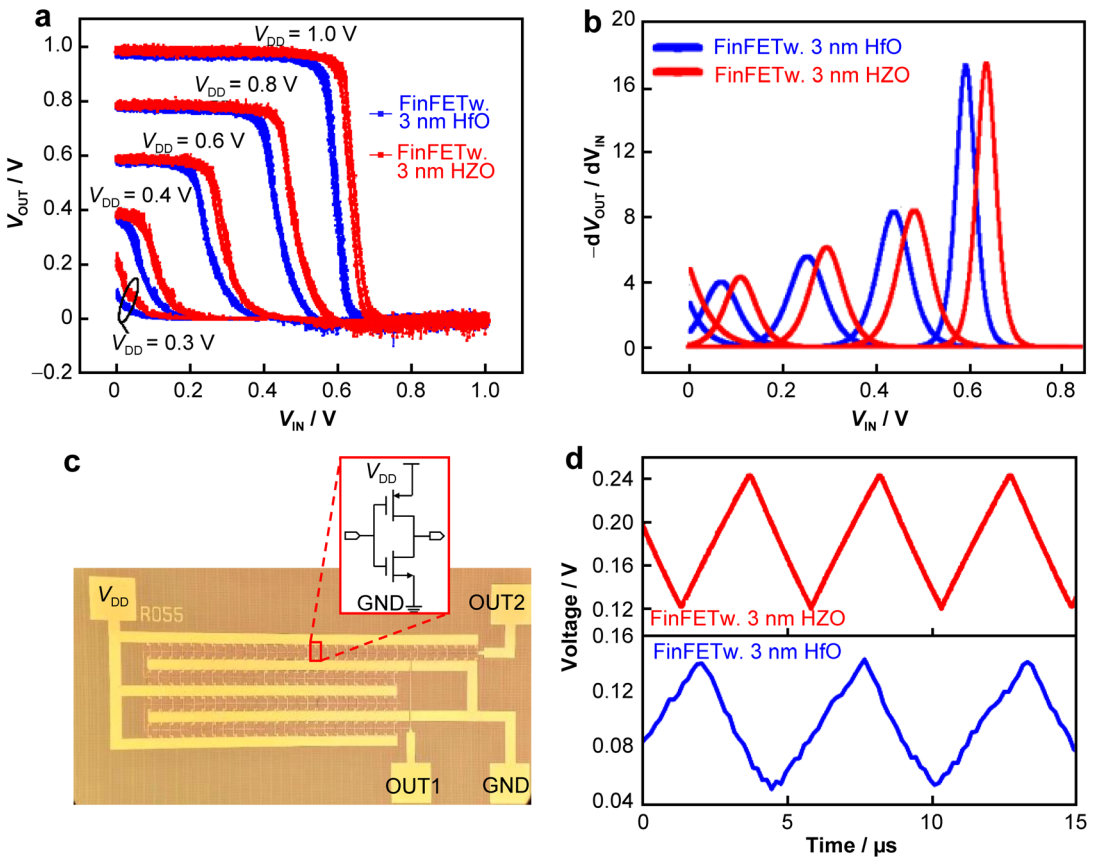

Fig. 5 **a** Voltage transfer curve of inverters based on FinFET with 3-nm HZO and HfO; **b** voltage gain of HZO-based-CMOS and HfO-based CMOS inverters; **c** optical images of ROs; **d** output waveforms of HfO-based FinFET and HZO-based FinFET 55-stage ring oscillators

FinFET circuits compared with those of circuits based on FinFET with 3 nm HZOs.

Conclusion

The ferroelectricity of ultra-thin 3-nm $Hf_{0.5}Zr_{0.5}O_2$ film is increased by our proposed approach that involves the use of an Al-doped TiN electrode. The CMOS HZO-based FinFETs with Al-doped stacks show clear N-DIBL and NDR characteristics. Furthermore, the I_{DS} values of HZO-based FinFETs were improved compared with those of a FinFET with 3 nm HfO_2. Enhanced performance (i.e., higher gain of inverters at low V_{DD}) was also confirmed in circuits based on HZO-based FinFETs, demonstrating the feasibility of these devices in ultra-low power applications.

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Declarations

Conflict of interests The authors declare that they have no conflict of interest.

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